Recent Test Results of GBCR3 @SLAC

Data Transmission Tests

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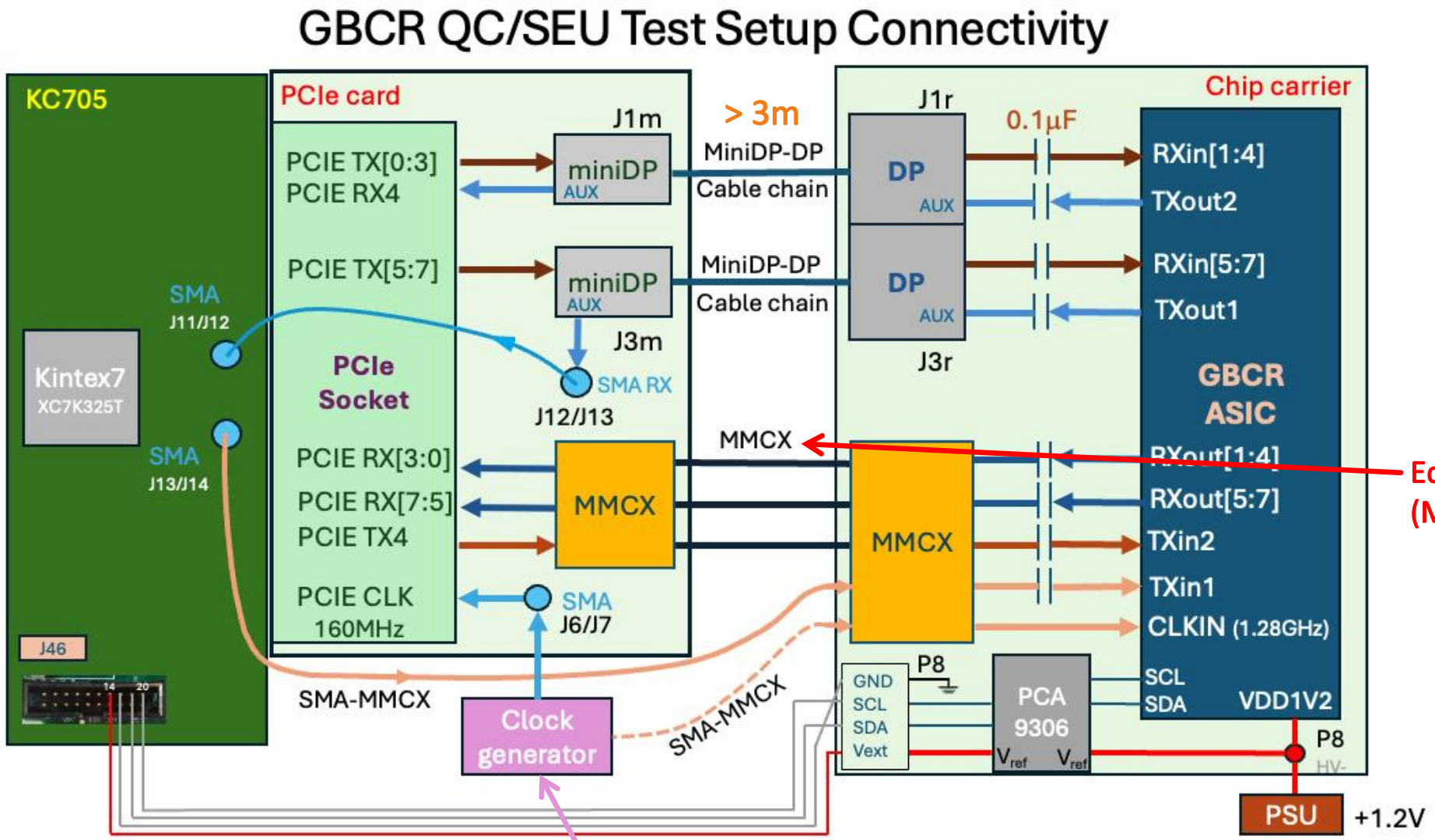
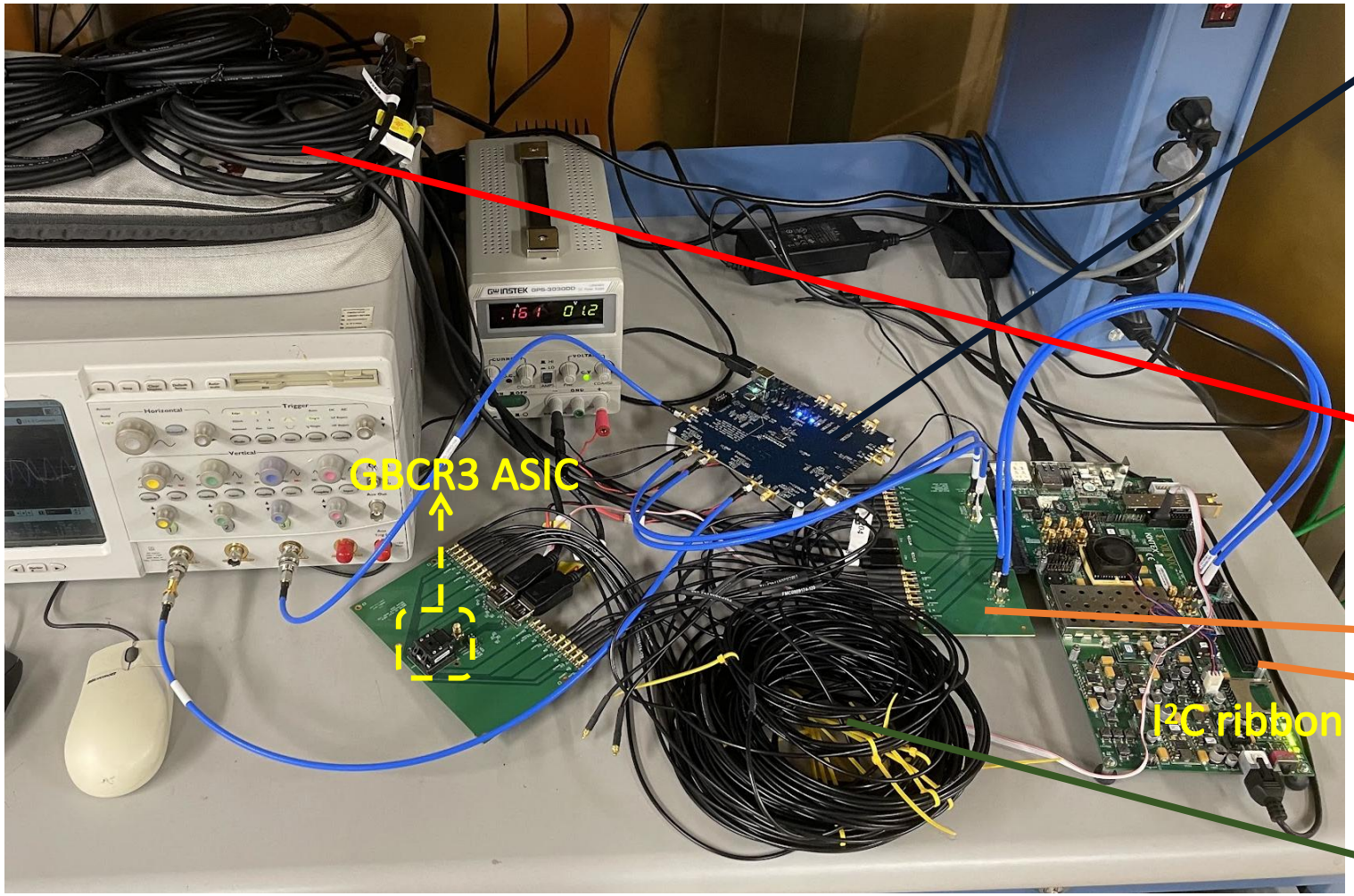
GBCR QC/SEU Test Readout Setup

Readout Platform



Test Setup @SLAC



Skyworks Si5344H for 160MHz Clock
(Also provide 1.28GHz clock output for GBCR retiming mode)

Si5338	→	Si5386	→	Si5344H
710MHz		wrong recommendation		current setup

miniDP-DP cables for twinax loss emulation
3 cables chained together
(~-19dB @ 640MHz)

PCIe card

Xilinx KC705

MMCX Cables for GBCR output link to PCIe card
- 1ft version for QC
- 10ft version for SEU

RX Channel Disable Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75

Disables RX channel when it is true

1st Test:
(GBCR3 C0073)

Disabled RX Channel	Status
1	Successful
2	Successful
3	Successful
4	Successful
5	All Other channels go wrong
6	Successful

2nd Test:
(GBCR3 C2328)

Disabled RX Channel	Status
1	Successful
2	Successful
3	Successful
4	Successful
5	All Other channels go wrong
6	Successful

Observations of Test Setup Behavior

- Sometimes one channel can stuck bad with large number of errors with no controlled fix other than power cycling.
  - Once in good mode, it is also quite stable and not easily disrupted into bad mode.
  - This feels like powerup random phase, scanning in the retiming mode may help.

Note:
Restart operation after setup change often has some staled old pipelined data which takes some time to flush before all channels getting into synch.

- Some patience to let system settle
- Short test runs to flush pipeline buffer

Retiming Mode Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

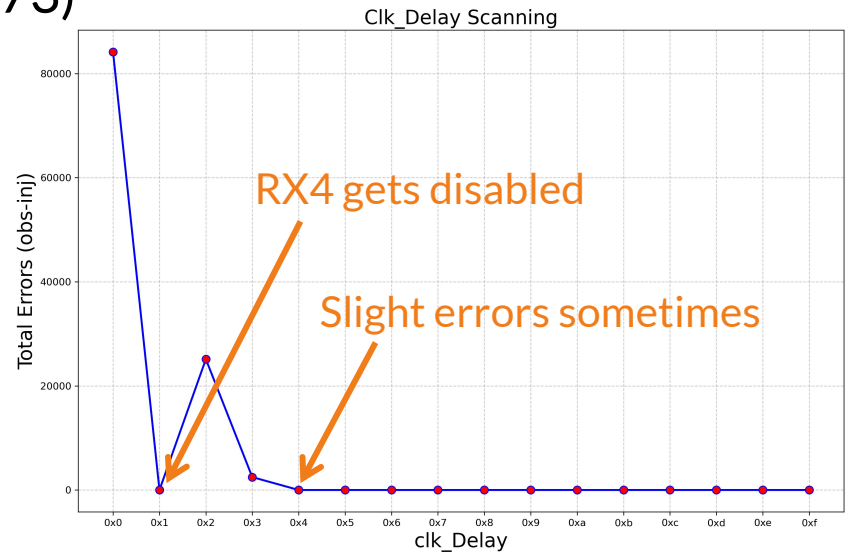
01111 for retiming mode

Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75

Scanning from 0x0 to 0xf

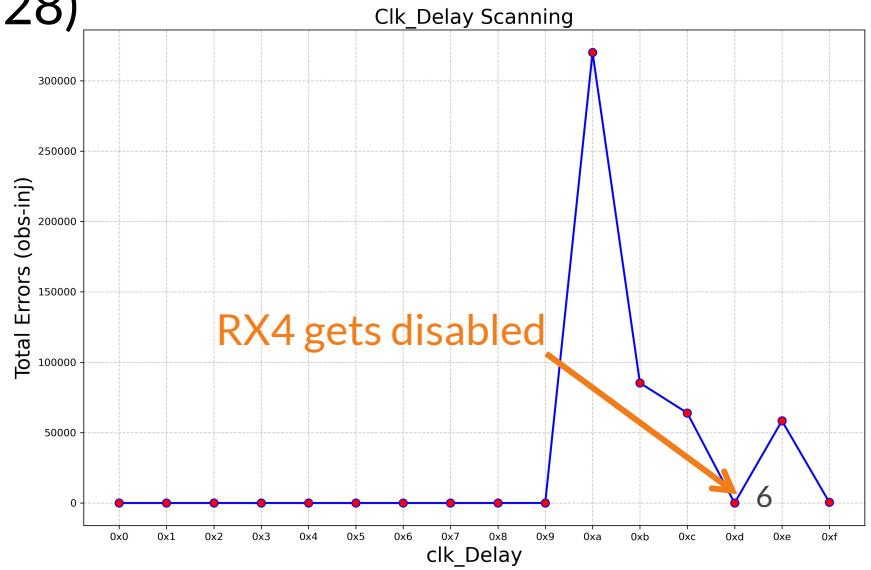
1st Test on RX4: (GBCR3 C0073)

~68.8% good phase points



2nd Test on RX4: (GBCR3 C2328)

~56.3% good phase points

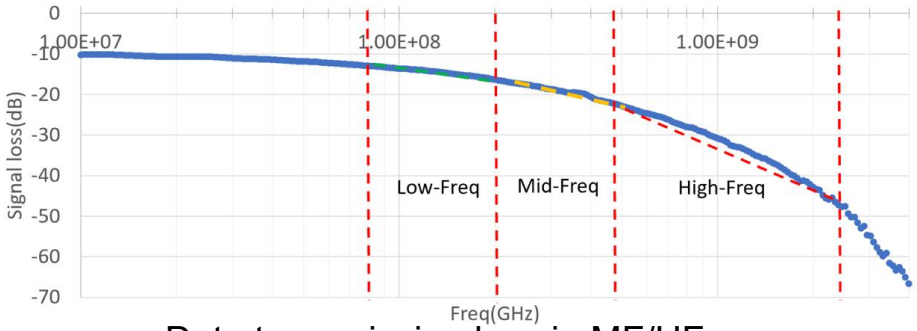


EQ Amplitude Factors Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

10111 for voted mode

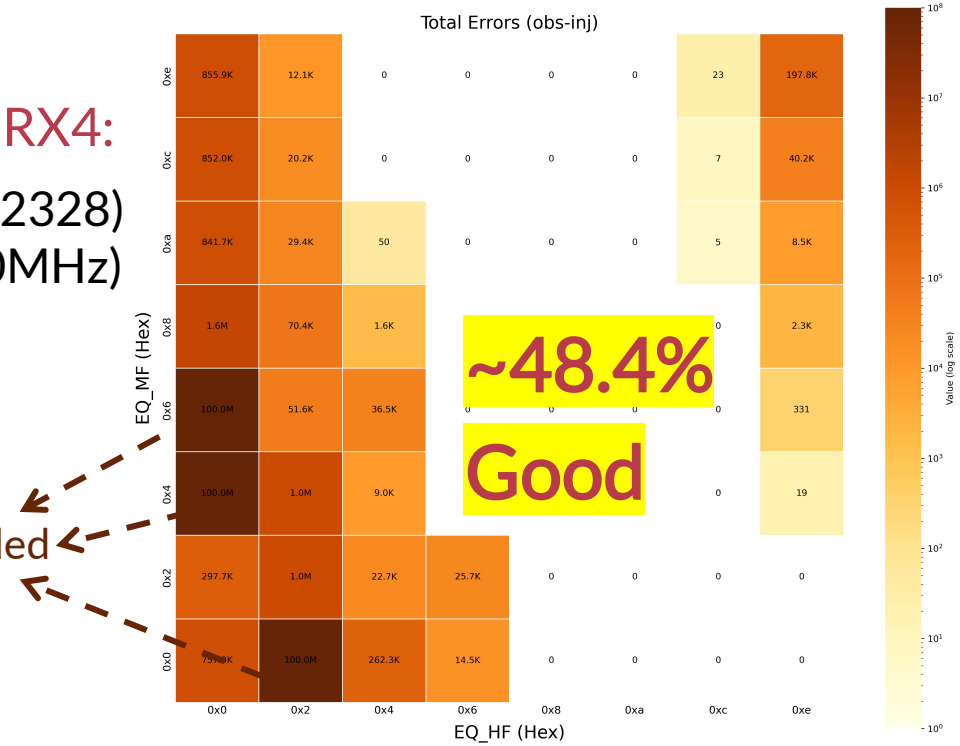
Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75



Data transmission loss in MF/HF range

➢ HF vs MF Scanning on RX4:

(GBCR3 C2328)
(loss ~19dB@640MHz)



~48.4%

Good

The channel gets disabled

Note: Scanning Step=2

I²C Readout Flakiness

Read back of 32x 8-bit registers, with ~23/500 times contained an error for a typical run.

Read 3 times to veto out fluctuations ?

```
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written !=  Read: [31, 136, 2, 31, 136, 136, 31, 136, 2, 31, 136, 2, 31
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
```

```
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written !=  Read: [31, 136, 2, 31, 31, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
```

```
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written !=  Read: [255, 136, 2, 31, 136, 2, 31, 136, 136, 31, 136, 2,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
Written ==  Read: [31, 136, 2, 31, 136, 2, 31, 136, 2, 31, 136, 2, 31,
```

Nearly all faulty cases can be characterized as a repeated value lingered on from previous register read, overtaking current register read value.

Summary

GBCR wiki-page:
https://twiki.cern.ch/twiki/bin/viewauth/Atlas/GBCR

- The disable RX channel function was tested and works properly for all channels except RX channel 5. The anomaly with disabling RX 5 requires further testing.
- The retiming mode of GBCR3 functions correctly, with approximately 70% of the parameter space operating normally, which may help find the good phase point.
- Parameter scanning results for HF vs MF show that approximately 50% of the parameter space related to EQ amp factors works properly.
- Power Cycling may power up random phase and cause some channel stuck in bad mode. (Is this connected to optoboard powerup instability observed by Bern?) Changing the fine delay in retiming mode may help.
- One should note that I^2C readout shows flakiness with ~4.6% error rate, primarily caused by previous register values persisting in subsequent reads.

Back ups

Connectivity details about the QC/SEU Test

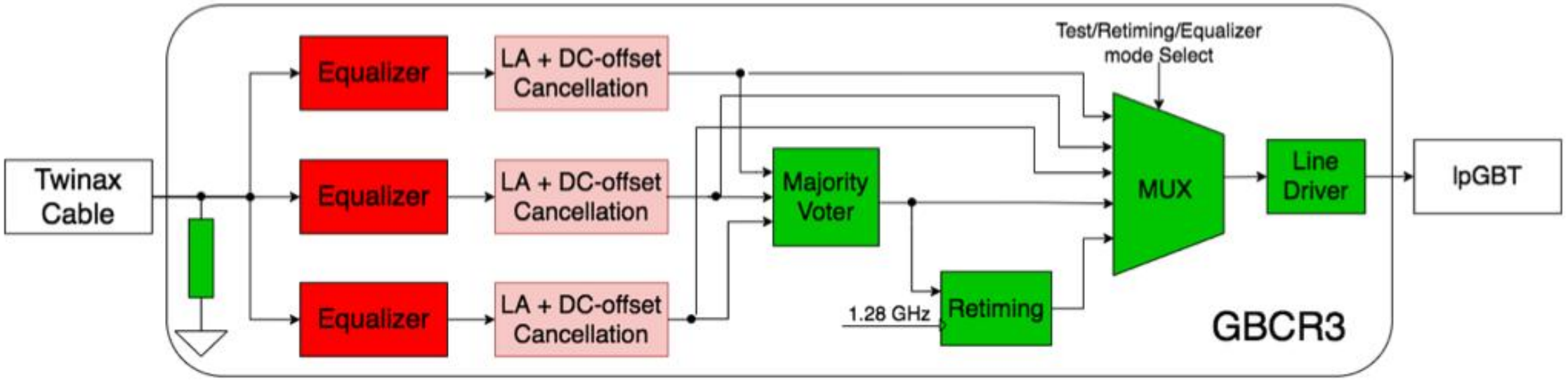
GBCR	Carrier DP			PCIe miniDP		PCIE socket			PCIE / FPGA	KC705 FPGA I/O			DAQ	KC705
signal	Conn	Channel		Conn	Channel	signal	Pin+	Pin-	Signal	Bank	Chan+	Chan-		SMA ports
RXin1	J1r	Lane 0	DP-miniDP cables	J1m	Lane 3	PER3	A29	A30	PCIE_TX3	116	P2	P1		
RXin2	J1r	Lane 1		J1m	Lane 2	PER2	A25	A26	PCIE_TX2	116	N4	N3		
RXin3	J1r	Lane 2		J1m	Lane 1	PER1	A21	A22	PCIE_TX1	116	M2	M1		
RXin4	J1r	Lane 3		J1m	Lane 0	PER0	A16	A17	PCIE_TX0	116	L4	L3		
RXin5	J3r	Lane 1		J3m	Lane 2	PER7	A47	A48	PCIE_TX7	115	Y2	Y1		
RXin6	J3r	Lane 2		J3m	Lane 1	PER6	A43	A44	PCIE_TX6	115	V2	V1		
RXin7	J3r	Lane 3		J3m	Lane 0	PER5	A39	A40	PCIE_TX5	115	U4	U3		
TXout2	J1r	Aux		J1m	Aux	PET4	B33	B34	PCIE_RX4 (pol flip)	115	V6	V5	Ch3	
TXout1	J3r	Aux		J3m	Aux	SMA RX bypass			USER_SMA_CLOCK	15	L25	K25	Ch8	SMA J11/12
	MiniDP-DP data lane polarity flip													
	MiniDP-DP AUX polarity no-flip													
	Carrier MMCX			PCIE MMCX		PCIE socket			PCIE / FPGA	KC705 FPGA I/O			DAQ	
	Pin+	Pin-		Pin+	Pin-	signal	Pin+	Pin-	Signal	Bank	Chan+	Chan-		
RXout1	J11	J10	MMCX coax	J32	J30	PET3	B27	B28	PCIE_RX3	116	T6	T5	Ch4	
RXout2	J9	J8		J35	J33	PET2	B23	B24	PCIE_RX2	116	R4	R3	Ch5	
RXout3	J4	J3		J31	J29	PET1	B19	B20	PCIE_RX1	116	P6	P5	Ch6	
RXout4	J2	J1		J28	J27	PET0	B14	B15	PCIE_RX0	116	M6	M5	Ch7	
RXout5	J24	J23		J40	J38	PET7	B45	B46	PCIE_RX7	115	AA4	AA3	Ch0	
RXout6	J22	J21		J42	J41	PET6	B41	B42	PCIE_RX6	115	Y6	Y5	Ch1	
RXout7	J20	J19		J39	J37	PET5	B37	B38	PCIE_RX5	115	W4	W3	Ch2	
TXin2	J15	J14		J36	J35	PER4	A35	A36	PCIE_TX4	115	T2	T1		
TXin1	J18	J17	MMCX->SMA bypass cable						USER_SMA_GPIO	12	Y23	Y24		SMA J13/14
CLKIN	J26	J25	<=Ext Clk			REFCLK	A13	A14	PCIE_CLK_Q0	115	U8	U7		
			1.28GHz retime			CLK_Q0	J6	J7						
						SMA ext sys clk 160MHz								
	MMCX connect + to +/- GBCR2/3													
	All RX signal symbol polarity flip													
	TX signal symbol polarity no-flip													

dis_MUX_BIAS Map

dis_MUX_BIAS<4:0> is used to select the output signal. (The default value of this signal is mistakenly inversed.) See table:

dis_MUX_BIAS<4:0>	Output signal
5'b01111	Retimed signal of voter
5'b10111	Voted signal
5'b11011	Equalizer signal A
5'b11101	Equalizer signal B
5'b11110	Equalizer signal C

Retiming Mode



- Retiming mode is crucial for reducing data jitter sent to lpGBT.

Data Frames

Word	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
7	Err	Channel ID			Time stamp																							
6	Time stamp																Inject error											
5	Inject error				EXPECTED CODE																							
4	EXPECTED CODE				RECEIVED CODE																							
3	RECEIVED CODE				Error position																							
2	Error position				Error counter																							
1	Error counter																											
0	CRC32																											

- Time Stamp : counter of 160 MHz clock
- Expected/Received code: BER PRBS7 or PRBS31 random 32 bit data/frame.
- Error position/counter: flagging and counting disagreeing bits in Received vs Expected comparison
- Inject error: deliberately inject wrong received data at regular intervals as keep_x0002_alive check signal
- CRC32: check sum