Recent Results of GBCR3 Testing @SLAC

Data Transmission Tests

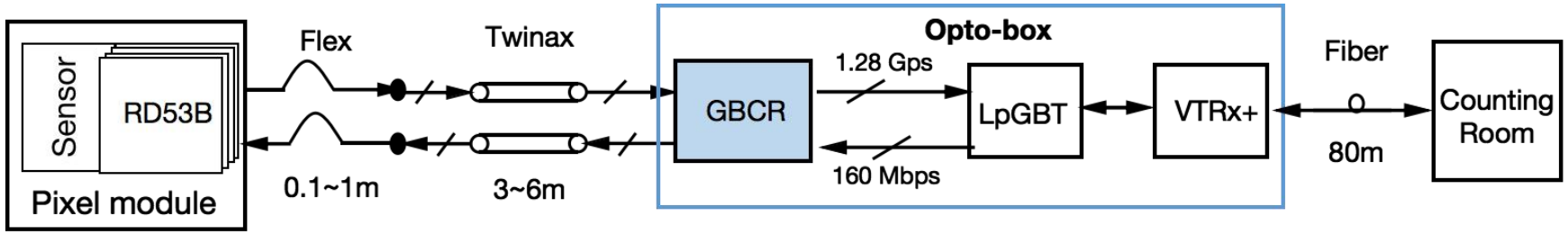
Dong Su, Andrew Young, Liangyu Wu
SLAC National Accelerator Laboratory
14 May 2025

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Introduction to the GigaBit Cable Receiver (GBCR) ASIC

- There are ~4500 GBCR chips in the ITk Pixel system:

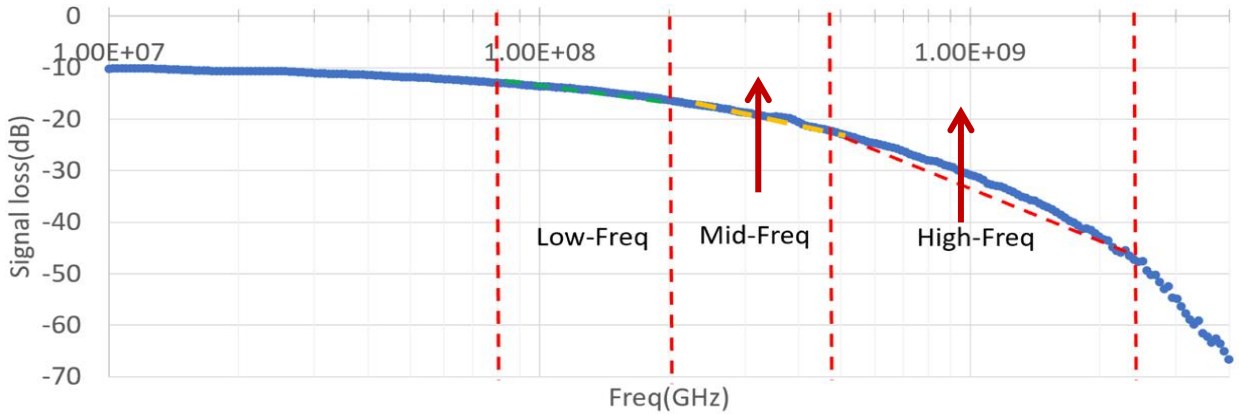


6 data links per GBCR

Zhang, L. and others JINST 18 (2023) 03, C03005

- Main Purpose:

To compensate for ITk pixel signal loss over 3-6m twinax Type-1 E-links at 1.28Gb/s.

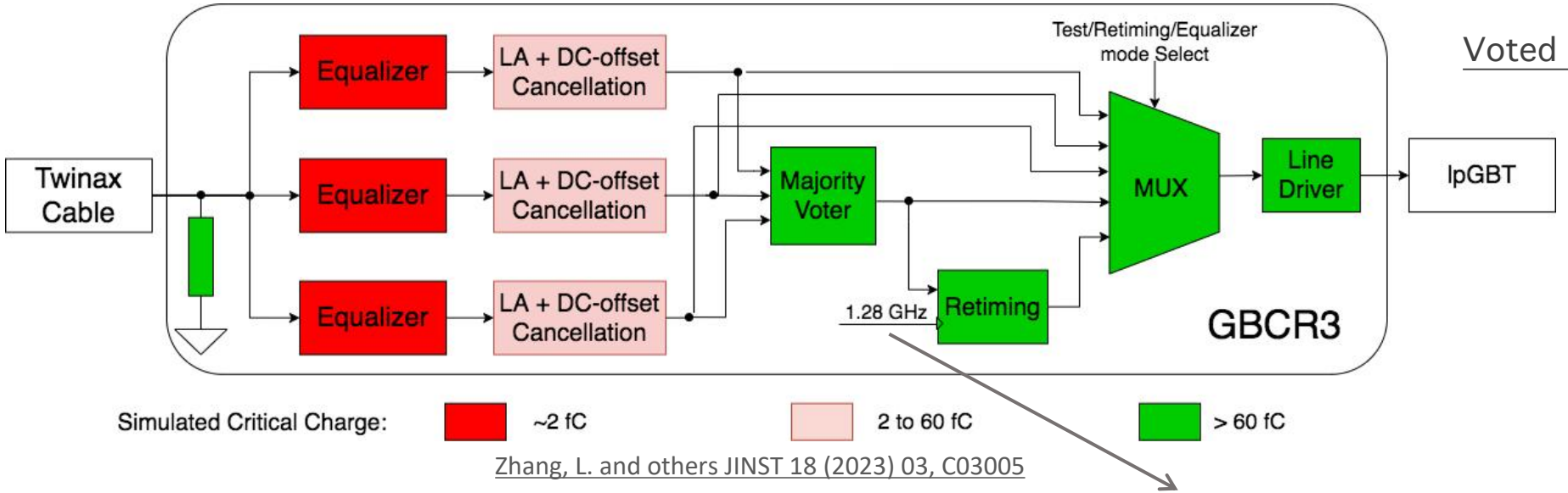


Boost the amplitude back

Data transmission loss in MF/HF range

Introduction to the GigaBit Cable Receiver (GBCR) ASIC

New EQ Logic Triplication in GBCR3



Voted mode VS Retiming mode

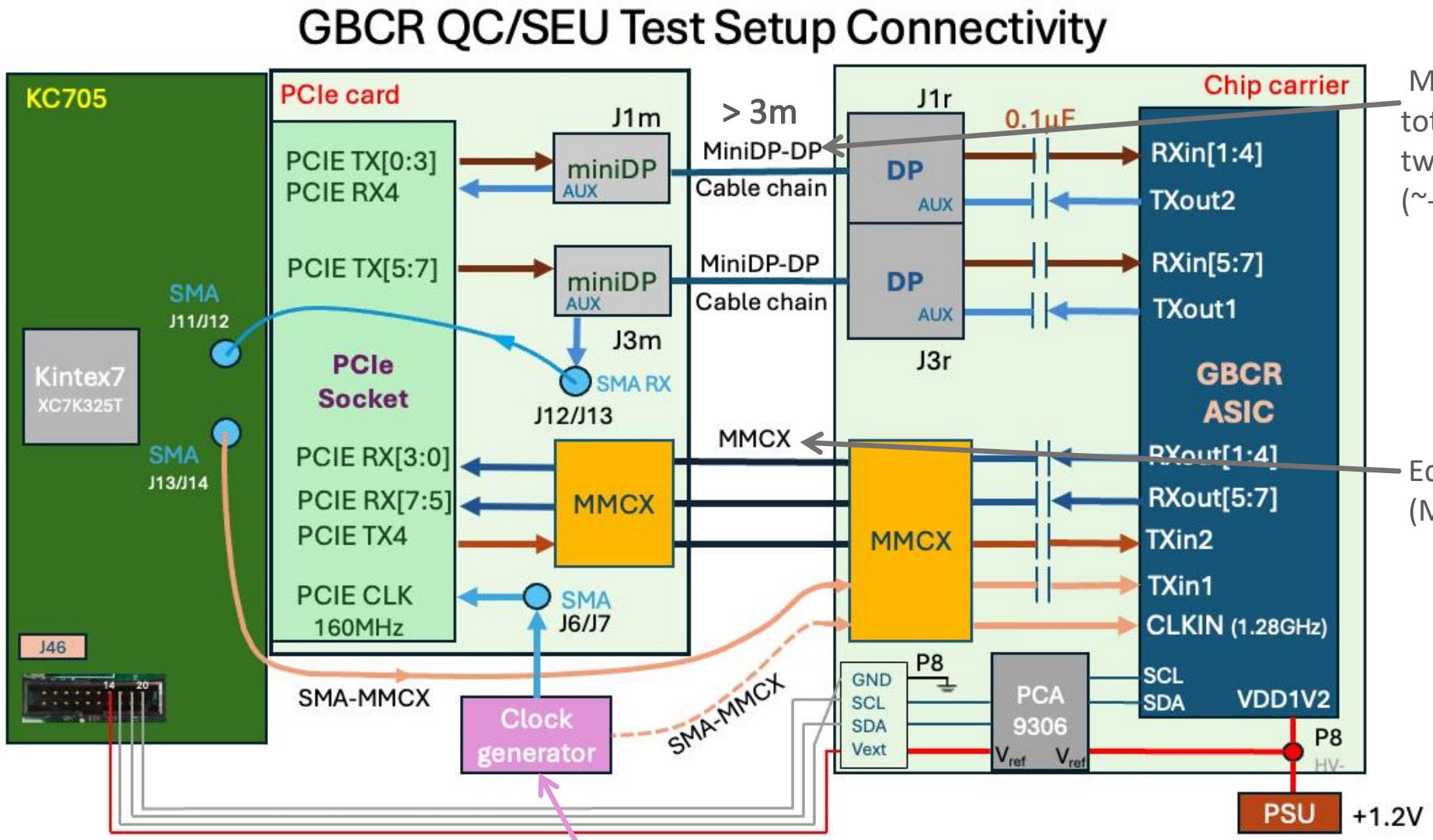
Zhang, L. and others JINST 18 (2023) 03, C03005

- Retiming mode is curial for **reducing data jitter** sent to lpGBT
- Using lpGBT's own 1.28GHz clock to rephase input data is the only way to control jitter (**drop jitter 288ps->94ps**)

See Zijun's Talk: here for more details

GBCR QC/SEU Test Readout Setup

Readout Platform



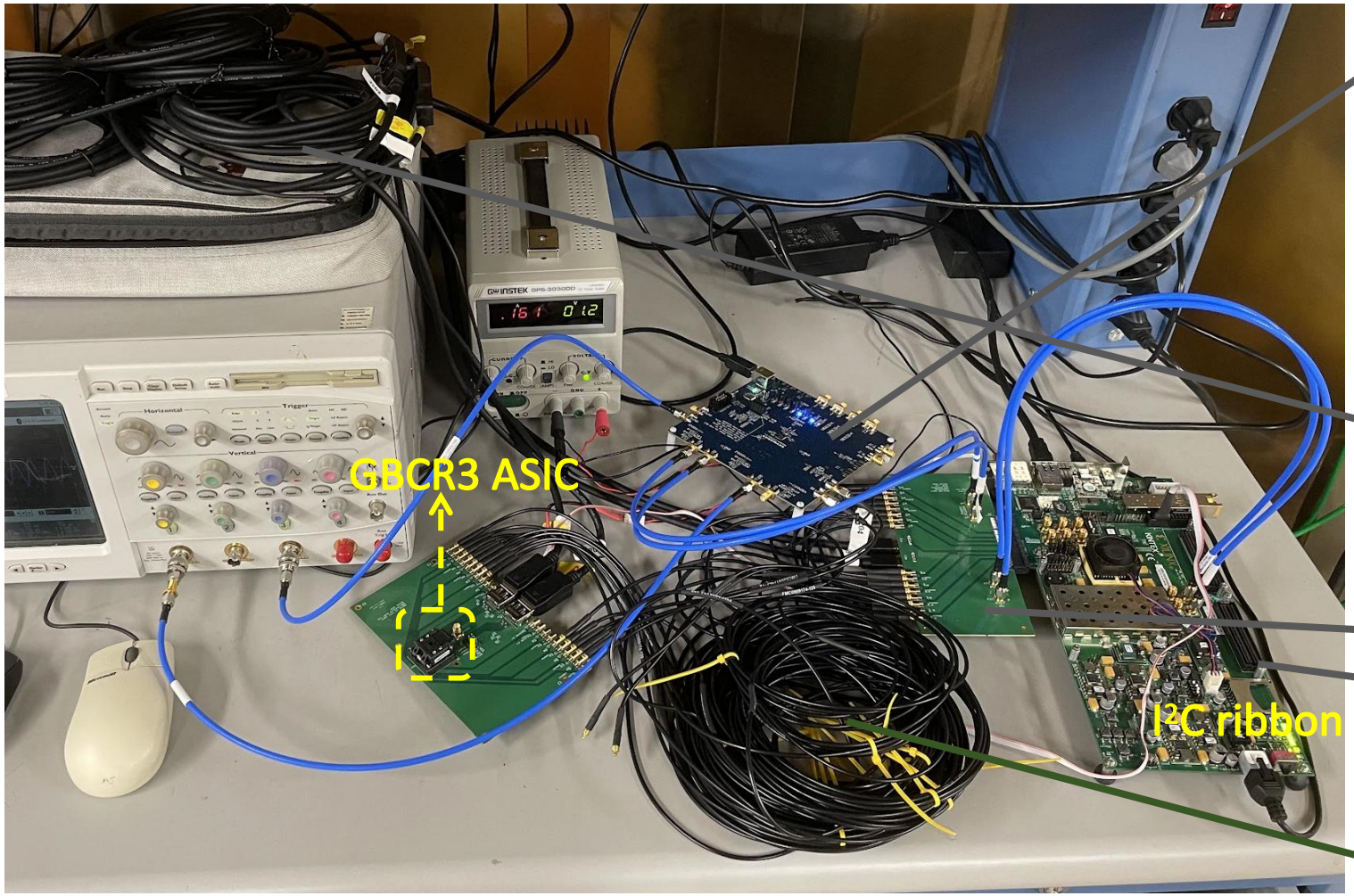
Mimicking realistic total Type0 flex+Type1 twinax cable loss (~-19dB @ 640MHz)

Equalized data output (MMCX RF coax cables)

I²C path

160MHz system clock by Skyworks Solutions

Test Setup @SLAC



Skyworks Si5344H for 160MHz Clock
(Also provide **1.28GHz clock output** for GBCR retiming mode)

Si5338 (710MHz) → Si5386 (wrong recommendation) → Si5344H (current setup)

miniDP-DP cables for twinax loss emulation
3 cables chained together
(~-19dB @ 640MHz)

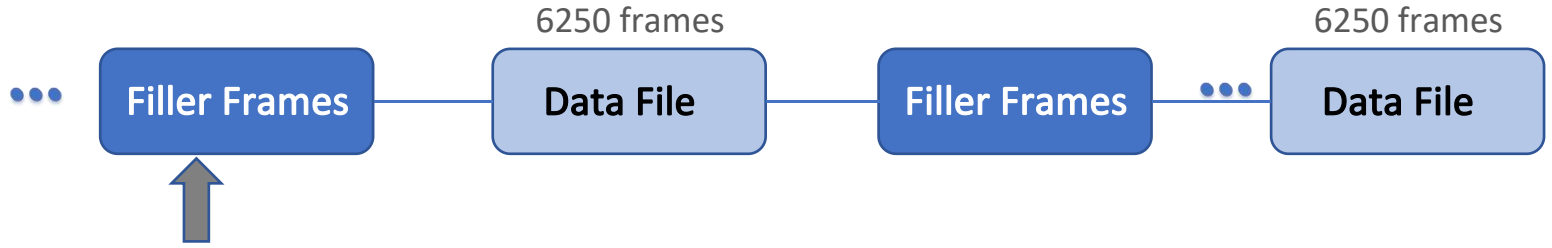
PCIe card

Xilinx KC705

MMCX Cables for GBCR output link to PCIe card
- 1ft version for QC
- 10ft version for SEU

General Dataflow Structure of the Setup

KC705 driven data files



Overall Statistics

Channels Breakdown

Run Summary

```
Files Summary:
File_num   Filler_Frames   Aligned_OK   Aligned_Err   NotAligned_Err   NotAligned_OK   Alignment_Loss   Bad_ChannelID   All_filler_files
60         374911          4            25            0                0               0                0               56

Channel Statistics Summary:
Channel   | Aligned OK | Aligned Error
-------------------------------------
0         | 0          | 5
1         | 0          | 0
2         | 0          | 0
3         | 0          | 0
4         | 0          | 5
5         | 0          | 5
6         | 0          | 5
7         | 0          | 5
8         | 4          | 0

Opened dump file: QAResults/2025-04-24_16-24-35/ChAll.TXT
End Run Summary

DAQ Lane   Nevt   Date time              Start / End            dT(min)   Start Inj/Obs   End Inj/Obs     Ninj/   Nobs
Ch0 RX5    5      2025-04-24 16:24:52     16:25:45              0.9       6754 / 6754     6758 / 6758     5 /     5
Ch1 RX6    0      -                      -                      -         -               -               -
Ch2 RX7    0      -                      -                      -         -               -               -
Ch3 TX2    0      -                      -                      -         -               -               -
Ch4 RX1    5      2025-04-24 16:24:52     16:25:45              0.9       6754 / 6753     6757 / 6757     5 /     5
Ch5 RX2    5      2025-04-24 16:24:52     16:25:45              0.9       6754 / 6754     6758 / 6758     5 /     5
Ch6 RX3    5      2025-04-24 16:24:52     16:25:45              0.9       6753 / 6753     6757 / 6757     5 /     5
Ch7 RX4    5      2025-04-24 16:24:52     16:25:45              0.9       6754 / 6754     6758 / 6758     5 /     5
Ch8 TX1    0      -                      -                      -         -               -               -

Summary written to QAResults/2025-04-24_16-24-35/summary.txt
line 52. All jobs are done!
```

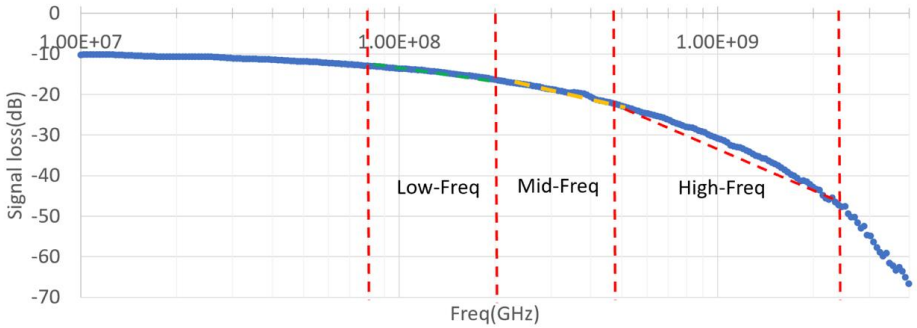
Deliberate error injection every 26-27s

EQ Amplitude Factors Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

10111 for **voted mode**

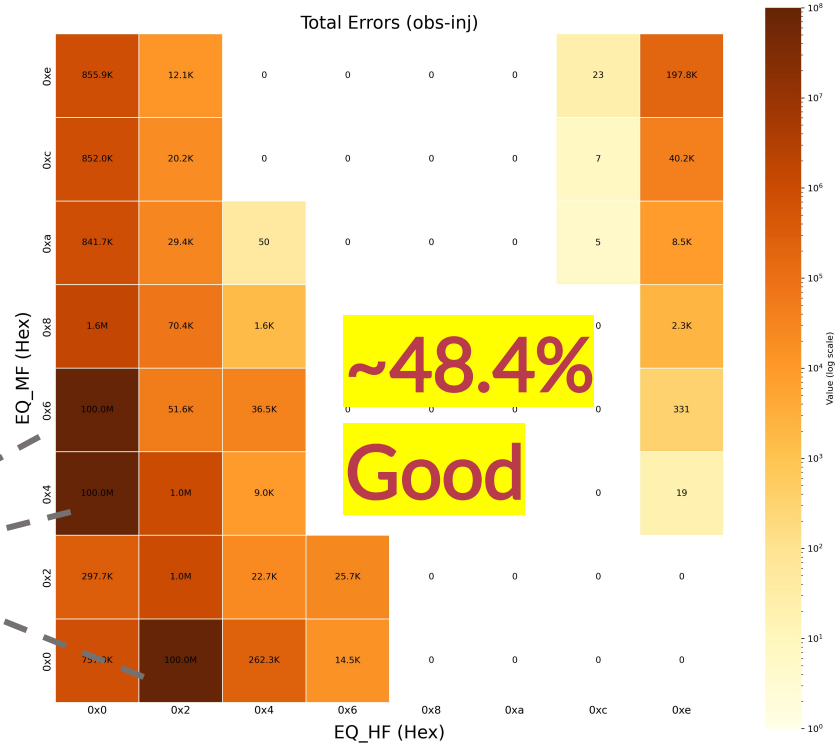
Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75



Data transmission loss in MF/HF range

HF vs MF Scanning on RX4:

(loss ~19dB@640MHz)



~48.4%

Good

The channel gets disabled

Note: Scanning Step=2

Retiming Mode Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

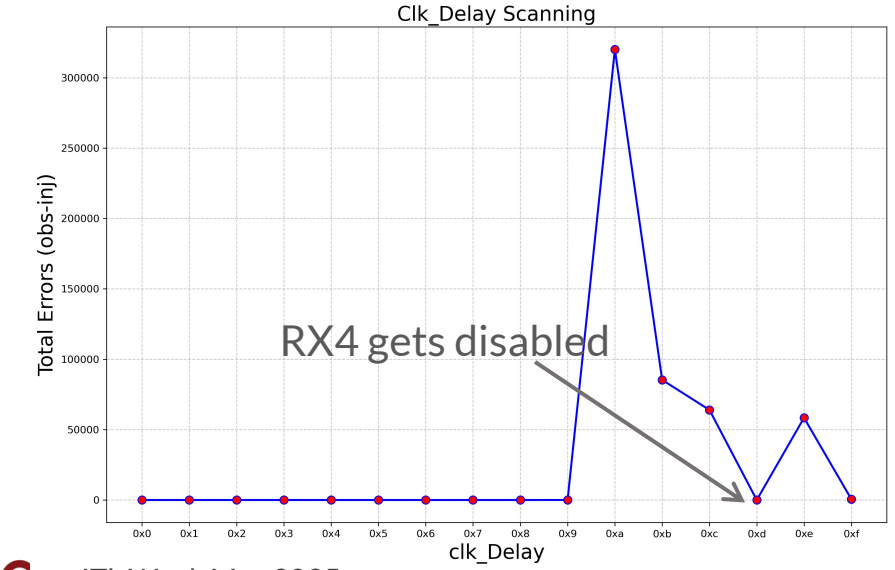
01111 for **retiming mode**

Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75

Scanning from 0x0 to 0xf

RX4 Channel:

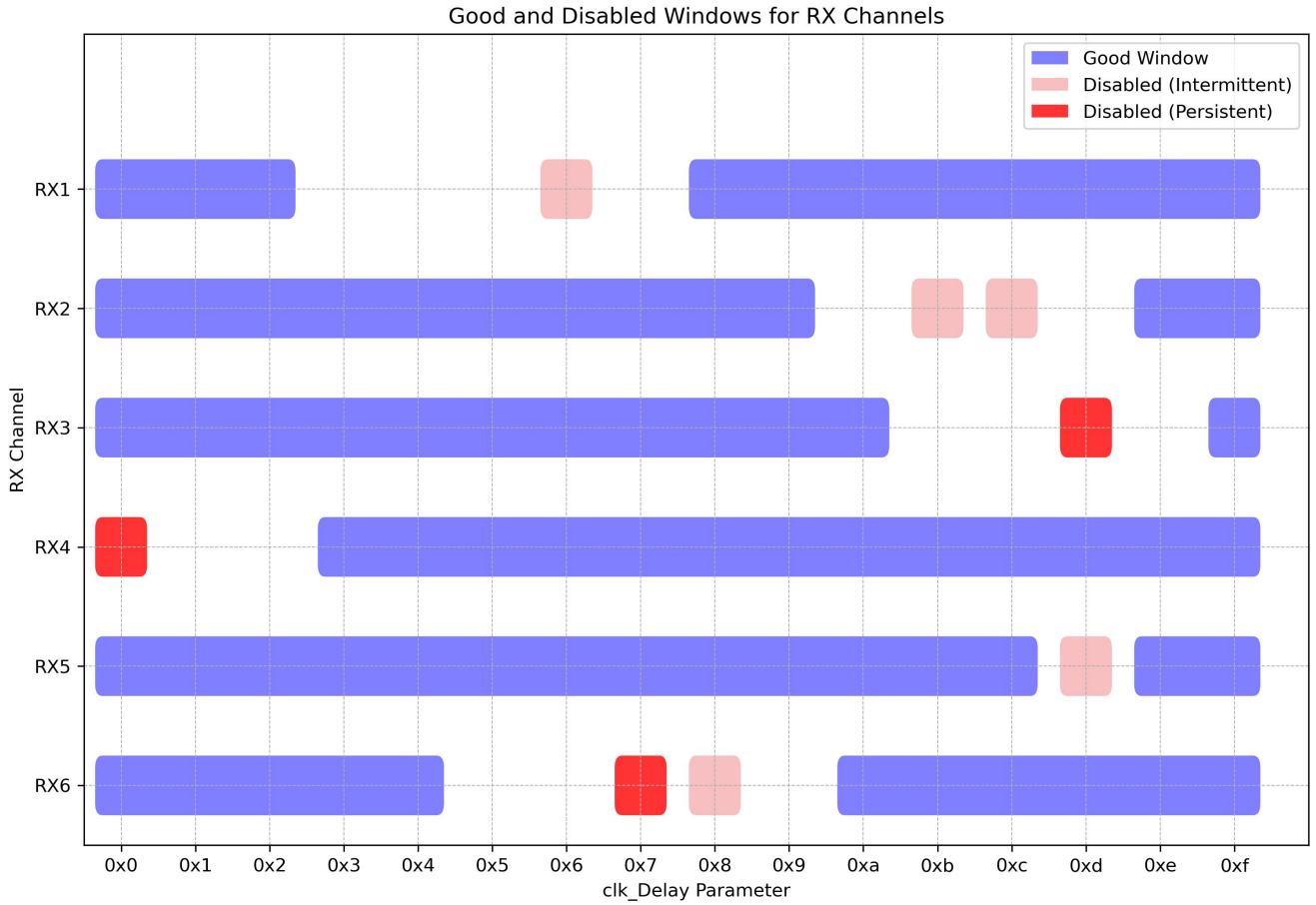
~56.3% good phase points



- Voted mode can occasionally leave channels in a bad state, needing KC705 power cycle to fix
- Using retime control to recover from bad state without power cycling would be ideal

Retiming Mode Test

A full scan of all RX channels for GBCR3 chip:



- Except for RX5, all RX channels show a wide range of good phase points, but at non-functional points, one or two parameters can disable the channel.
- For RX5, nearly all clk_Delay parameters allowed proper function, making it unclear if these parameters were indeed altered.
- Reloading firmware will change the absolute position of the good window for the same RX channel.

Retiming Mode & Voted Mode Correlation Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75

Retiming mode/Voted mode

To check whether the voted&retiming mode could operate independently:

- Ran retiming mode with specific clk_Delay parameters for 6 runs, then switched to voted mode for 6 more runs.
- For all the channels, results showed voted mode operates independently of retimed mode.

RX Channel Disable Test

Each RX channel has 4x 8-bit registers (6 RX channels in total for GBCR3)

Reg	7	6	5	4	3	2	1	0	Default
0		dis_Ch_BIAS	dis_LPF_BIAS	dis_MUX_BIAS					0x17
1	EQ_HF1				EQ_HF2				0xbb
2	EQ_HF3				EQ_MF				0xbb
3	dis_EQ_LF	AmpSel			clk_Delay				0x75

Disables RX channel when it is true

Double-Checks

Disabled RX Channel	GBCR3 C0073	GBCR3 C2328
1	Successful	Successful
2	Successful	Successful
3	Successful	Successful
4	Successful	Successful
5	All Other channels go wrong	All Other channels go wrong
6	Successful	Successful

- Swapping test shows we can successfully disable RX5 channel

Summary

- Parameter scanning results for HF vs. MF show that about 50% of EQ amp factor choices yield a good and stable transmission.
- The retiming mode of GBCR3 functions correctly, with approximately 70% of the parameter space operating normally, which could help find the good phase point.
- Tests verified that the retiming and voted modes of the GBCR3 chip can operate independently without interference. Further validation is needed for adjusting the clk_delay parameters in RX5 channel's retiming mode.
- The disable RX channel function was tested and works properly for all channels except RX channel 5. There are indications that this anomaly may not be related to the chip itself, further testing is required.

GBCR wiki-page:
https://twiki.cern.ch/twiki/bin/viewauth/Atlas/GBCR

Back ups

Connectivity details about the QC/SEU Test

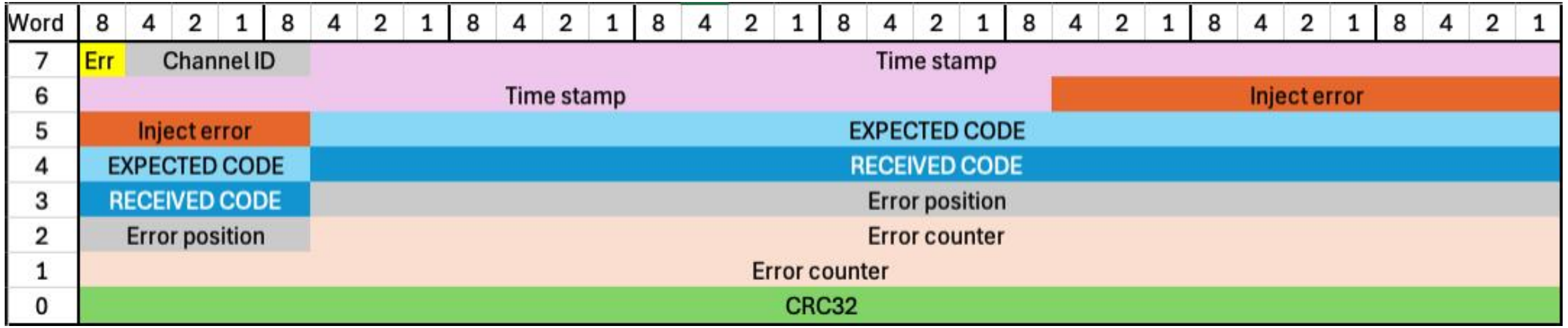
GBCR	Carrier DP			PCIe miniDP		PCIE socket			PCIE / FPGA	KC705 FPGA I/O			DAQ	KC705
signal	Conn	Channel		Conn	Channel	signal	Pin+	Pin-	Signal	Bank	Chan+	Chan-		SMA ports
RXin1	J1r	Lane 0	DP-miniDP cables	J1m	Lane 3	PER3	A29	A30	PCIE_TX3	116	P2	P1		
RXin2	J1r	Lane 1		J1m	Lane 2	PER2	A25	A26	PCIE_TX2	116	N4	N3		
RXin3	J1r	Lane 2		J1m	Lane 1	PER1	A21	A22	PCIE_TX1	116	M2	M1		
RXin4	J1r	Lane 3		J1m	Lane 0	PER0	A16	A17	PCIE_TX0	116	L4	L3		
RXin5	J3r	Lane 1		J3m	Lane 2	PER7	A47	A48	PCIE_TX7	115	Y2	Y1		
RXin6	J3r	Lane 2		J3m	Lane 1	PER6	A43	A44	PCIE_TX6	115	V2	V1		
RXin7	J3r	Lane 3		J3m	Lane 0	PER5	A39	A40	PCIE_TX5	115	U4	U3		
TXout2	J1r	Aux		J1m	Aux	PET4	B33	B34	PCIE_RX4 (pol flip)	115	V6	V5	Ch3	
TXout1	J3r	Aux		J3m	Aux	SMA RX bypass			USER_SMA_CLOCK	15	L25	K25	Ch8	SMA J11/12
	MiniDP-DP data lane polarity flip													
	MiniDP-DP AUX polarity no-flip													
	Carrier MMCX			PCIE MMCX		PCIE socket			PCIE / FPGA	KC705 FPGA I/O			DAQ	
	Pin+	Pin-		Pin+	Pin-	signal	Pin+	Pin-	Signal	Bank	Chan+	Chan-		
RXout1	J11	J10	MMCX coax	J32	J30	PET3	B27	B28	PCIE_RX3	116	T6	T5	Ch4	
RXout2	J9	J8		J35	J33	PET2	B23	B24	PCIE_RX2	116	R4	R3	Ch5	
RXout3	J4	J3		J31	J29	PET1	B19	B20	PCIE_RX1	116	P6	P5	Ch6	
RXout4	J2	J1		J28	J27	PET0	B14	B15	PCIE_RX0	116	M6	M5	Ch7	
RXout5	J24	J23		J40	J38	PET7	B45	B46	PCIE_RX7	115	AA4	AA3	Ch0	
RXout6	J22	J21		J42	J41	PET6	B41	B42	PCIE_RX6	115	Y6	Y5	Ch1	
RXout7	J20	J19		J39	J37	PET5	B37	B38	PCIE_RX5	115	W4	W3	Ch2	
TXin2	J15	J14		J36	J35	PER4	A35	A36	PCIE_TX4	115	T2	T1		
TXin1	J18	J17	MMCX->SMA bypass cable						USER_SMA_GPIO	12	Y23	Y24		SMA J13/14
CLKIN	J26	J25	<=Ext Clk			REFCLK	A13	A14	PCIE_CLK_Q0	115	U8	U7		
			1.28GHz retime			CLK_Q0	J6	J7						
						SMA ext sys clk 160MHz								
	MMCX connect + to +/- GBCR2/3													
	All RX signal symbol polarity flip													
	TX signal symbol polarity no-flip													

dis_MUX_BIAS Map

dis_MUX_BIAS<4:0> is used to select the output signal. (The default value of this signal is mistakenly inversed.) See table:

dis_MUX_BIAS<4:0>	Output signal
5'b01111	Retimed signal of voter
5'b10111	Voted signal
5'b11011	Equalizer signal A
5'b11101	Equalizer signal B
5'b11110	Equalizer signal C

Data Frames



- Time Stamp : counter of 160 MHz clock
- Expected/Received code: BER PRBS7 or PRBS31 random 32 bit data/frame.
- Error position/counter: flagging and counting disagreeing bits in Received vs Expected comparison
- Inject error: deliberately inject wrong received data at regular intervals as keep_x0002_alive check signal
- CRC32: check sum